1. (20 points) In the Logicly logic simulator, wire up the edge-triggered D flip-flop shown in the figure below. This is a more practical flip-flop that the one we first saw in class. It is clocked, which means the timing is synchronized to an external source which is usually a fixed-frequency square wave. Note: use a switch for the D input, and a “clock” for the CLK input. To animate the simulation, use the play button in the upper right of the screen. There is also a step-forward button which may also be helpful. Discuss the following points:

(a) How does each input effect the value of Q?

(b) If you change the input state D, when does the output change? Is it as the clock goes from low to high, as the clock goes from high to low or at some other time?

(c) How long after D changes does the value of Q change? Is this consistent with your answer to the first part? Explain why this might be useful in a circuit. Think of a computer example, do you always know exactly when a user will press a key?

(d) The D flip flop most commonly serves to delay the D signal, which is one type of memory. How long is the delay, what determines the length of the delay?